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Using Time-Based Control Techniques for Active Rectification

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Abstract

As power converters are ever decreasing in size, ways of controlling power switches fast, reliable and efficient is needed. Using time-based control techniques on integrated circuits benefits in area, power and speeds. In this poster we propose new topologies for active rectification in high and very high frequency resonant converters. These topologies involve both phase-locked and delay-locked loops to achieve zero-voltage switching rectifiers. The delay-locked loop topology is a 1st order circuit, and thus inherently stable and easy to implement. The largest advantage of these topologies is removing the requirements for high power diodes in very high frequency applications.

Brief Description and Figures

To decrease the size of power converters, the typical approach is to increase the switching frequency. However, increasing the switching frequency also increases switching losses. A solution to this is to use resonant power converters, with inherent zero-voltage and/or zero-current switching (ZVS and ZCS, respectively). This allows an increase in switching frequency, minimizing the size of the passive storage devices, while still keeping the switching losses low. A resonant power converter is often implemented as an inverter and a rectifier. A schematic of a class DE rectifier is shown in Fig. 1. The resonant inverter is seen as a sinusoidal current source. The rectifier can operate purely with diodes but is here illustrated with synchronous transistors.

The current stresses on the diodes shown in this topology is high. It is thus not suited for medium to high power ranges due to the limited availability of diodes operating both at VHF and with high currents. To address this issue, synchronous transistors can be implemented as per Fig. 1. However, a problem is ensuring ZVS and ZCS. The delay through both gate drivers and level shifters can be in the range of 5-15ns – a significant parts of a period in a VHF converter. Using time-based control techniques and feedback we can implement 'negative' delay, to achieve ZVS and ZCS. Fig 2. and Fig. 5. shows two such concepts, and Fig 3. and Fig. 6. shows their respecting waveforms.

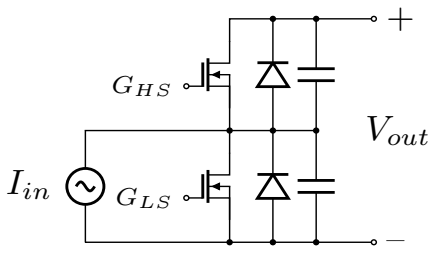

Fig. 1 - Class DE Rectifier with Sinusoidal Input Current

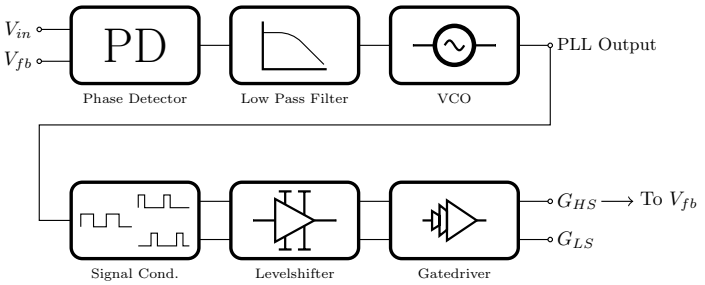

Fig. 2 - Concept of PLL Controlled Rectifier

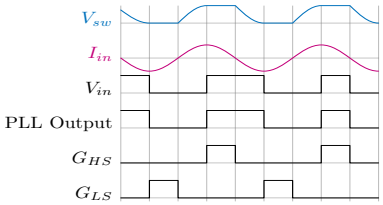

Fig. 3 - Timing of PLL Driven Rectifier - PLL in Lock

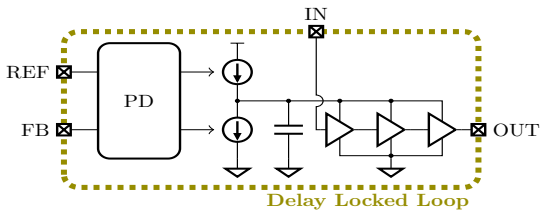

Fig. 4 - Schematic of a Delay Locked Loop

The phase-locked loop (PLL) controller shown in Fig. 2 consist of a PLL with a phase detector, a low pass filter and a voltage-controlled oscillator (VCO). The output of the PLL is fed to a signal conditioning block, which handles duty cycle and deadtime. These signals are fed through pulse triggered level shifters [4] and gate drivers to their respective gates. When the PLL is in lock it ensures ZVS of the HS FET. As the PLL is a second-order system, stability can be a challenge to achieve. In Fig. 3 the signals of the PLL controller in locked mode is shown. This has previously been implemented in systems for wireless power transfer [2].

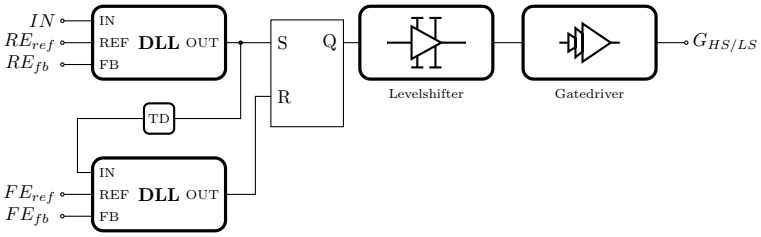

Fig. 5 - Concept of a Single Switch DLL Control Loop

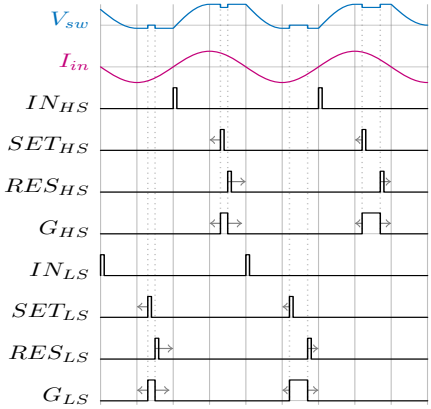

Fig. 6 – Timing of DLL During Locking

The delay-locked loop (DLL) control-loop (Fig. 5.) is more complex, as it requires two DLLs (Fig. 4), a SR latch and level shifter plus gate driver per switch. Only the setup for a single switch is shown in Fig. 5. Two of these control loops is thus necessary for the rectifier show in Fig. 1. Each DLL controls the rising and falling edge of the FETs respectively. It is similar to the structure used in [3] for ZVS and ZCS of a piezoelectric element. The DLL is a first-order system, and thus inherently stable.

In Fig. 6. the signals in the DLL controlled rectifier are shown. The set/reset pulses for the SR latch is controlled by their respective DLLs, to ensure ZVS and ZCS. By controlling the starting delay in the DLLs and their following respective increase/decrease in delay, we can ensure close to ZVS / ZCS without risking shoot-throughs or hard-switching. When the DLL is in lock, the signals are identical to that of the PLL in lock, seen in Fig. 3.

Key Contributions

Two control topologies for active rectification have been presented. The use of PLLs and DLLs in the control loop can ensure ZVS and ZCS, and minimize the requirement for high speed, high current carrying diodes. The DLL, while containing more design blocks, are inherently stable, and thus easier to implement. Furthermore, these topologies, together with the power stage, are all CMOS compatible, and thus fully integrable allowing for smaller packaging.

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